W Band Monolithic Multipliers

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Abstract

This paper describes the realization of a W band planar monolithic multiplier using finite ground coplanar lines. These lines provide near TEM low loss propagation to W band and enhance multiplier performance. The developed MMIC multipliers have demonstrated 93 mW output power, 26% efficiency and output bandwidth from 70 to 80 GHz.

Introduction

Local oscillator sources are an important part of all high frequency receiver applications. These sources have a long experimental history mostly based on Schottky barrier diodes. Early diodes were honeycomb anode chips with a whisker contact and were characterized by very small parasitics. However, they were difficult to handle, have problems with thermal cycling and vibrations and have performance that is critically dependent on the shape of the whisker. Even with these problems, whisker contacted multipliers were the most common millimeter and submillimeter wave sources until the late 1980s. In 1987 Bishop et. al. proposed the microchannel structure as an alternative high frequency planar diode [1]. This structure was much easier to handle and mount in waveguide blocks. Furthermore, the structure could also be used to fabricate multiple diodes for the same mount. An example of this type of device is given by Rizzi et.al. [2] with the multiplier having a peak output of 55 mW at 174 GHz, and an efficiency of 25% with an output of 37 mW using a balanced combination of two diode pairs.

Presently most millimeter wave multipliers are of waveguide type. Waveguide circuits have the lowest loss and highest Q needed for efficient multiplier operation. Furthemore, they can include tuners and backshorts needed to optimize for peak performance. However, waveguide mounts are complex to design and fabricate, and become more difficult and expensive to machine with increasing frequency and smaller size. MMIC multipliers have many advantages compared to waveguide structures. They can provide low cost and small size circuits, while large numbers can be fabricated at the same time using integrated circuit fabrication techniques. However, planar multipliers have some limitations. They exhibit higher loss and lower Q than the waveguide ones. It is also much more difficult to include tuning elements. Even with these limitations, some very useful MMIC multipliers have been reported. Chen et. al. [3] described a planar MMIC multiplier with an output power of 65 milliwatts and an efficiency of 25% at 94 GHz using a microstrip circuit.

Microstrip and coplanar waveguides are two guiding structures that are used extensively for high frequency MMIC applications. One problem associated with the microstrip approach is that line characteristics depend on the substrate thickness and moding can occur at high frequencies unless the substrate is thinned. CPW has a performance which is less dependent on the substrate thickness, but problems can occur because of parasitic parallel plate waveguide modes which can only be suppressed by use of via holes. However, the via holes make circuit fabrication more difficult and can cause additional problems if placed incorrectly. The more complex propagation properties add to circuit design problems since complicated line models are needed to correctly predict results.

This paper describes circuits fabricated by use of a modified coplanar waveguide structure with finite width ground planes. This Finite Ground Coplanar (FGC) line overcomes many of the problems associated with conventional CPW and microstrip line, and can be scaled easily to higher frequencies. The narrow ground planes reduce the effect of parallel plate modes thus eliminating the need for via holes. Wafer thinning is not required and the back side metallization does not

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affect line characteristics. The line geometry is chosen so that the width of the entire structure is less than half the dielectric wavelength at the highest frequency under consideration. The loss normalized to wavelength has an inverse square root dependence indicating an ohmic nature. The loss is approximately 0.25 dB/mm at 100 GHz. The measured data was fitted to a lossy TEM transmission line model using LIBRA. There is a close fit between the measured and modeled results, again indicating that FGC line can be correctly described by a non-dispersive lossy TEM line. A detailed description of these lines is given by Brauchler[3].

Design of FGC Multipliers

The FGC line elements are used as a starting point for the multiplier design. Experimental measurements gave a range of 20 to 80 Ω for line impedances. A nonlinear multiple reflection program was used to design the multiplier [4]. In a conventional multiplier design, the varactor diode is usually specified and the multiplier is designed around it. Here, the diode parameters become part of the design process. The operating frequency sets the doping level, and the peak RF voltage swing, limited by the breakdown voltage, sets the active epitaxial layer width. The multiplier bias point is also a parameter. Multiplier operation varies from a resistive mode, where the input Q at the pump frequency is in the range from 1 to 2 and the efficiency is modest, to a reactive mode where the input Q and the efficiency are both higher. The realized impedance for high Q as compared to the design impedance is more sensitive to small changes in element values than similar low Q topologies. Waveguide multipliers can be designed for higher Q, with modest differences in the designed vs. realized impedances, adjusted with tuners and backshorts. Similar impedances in an MMIC multiplier are fixed, with the bias point being the only available "tuning". The multiple reflection code was modified to adjust the diode area and bias so that the required embedding impedances could be realized with FGC lines and the input Q was approximately two.

Results and Discussions

A variety of multipliers including series and shunt diodes and single and multiple diodes were designed, fabricated and tested. The best results, which have been obtained with the diode pair shunt structure, will be described here. A photograph of the multiplier is shown in Figure 1 with a close up view of the diodes shown in Figure 2. It is designed with 50 Ω input and outputs on the ends, a second harmonic trap on the input side and a fundamental trap on the output sides. The varactor diodes are connected to the signal line with inductive lines. The multiplier is evaluated using on wafer probing at the input and output ports. The input and output measurements are calibrated to the tips of the probes using Ka band and W band HP 8510 test sets and with power meters at the pump and output frequencies. A Ka band TWT is used as the source. This combination of input and output test set frequencies limited the output frequency range to 70 to 80 GHz. The measured output power and efficiency of the multiplier is shown in Figure 3. The first design iteration provided a multiplier with peak efficiency equal to 16.3 % and peak output power equal to 72 mW at 80 GHz. The design worked well over the entire measurement frequency range. The efficiency and return loss from 70 to 80 GHz for a constant 100 mW input power are shown in Figure 4. The -3 dB efficiency bandwidth is wider than the 10 GHz measurement bandwidth. A second iteration of this multiplier provided an output power of 93 mW. The design efficiency of this multiplier was 32%. The estimated loss of the input and output circuits based on line measurements was 1.1 dB and the return loss at the peak efficiency point was -7.5 dB. The resulting multiplier internal efficiency is 26%, in reasonable agreement with the model prediction. This output power level is among the best reported for MMIC multipliers at W band.

Acknowledgements

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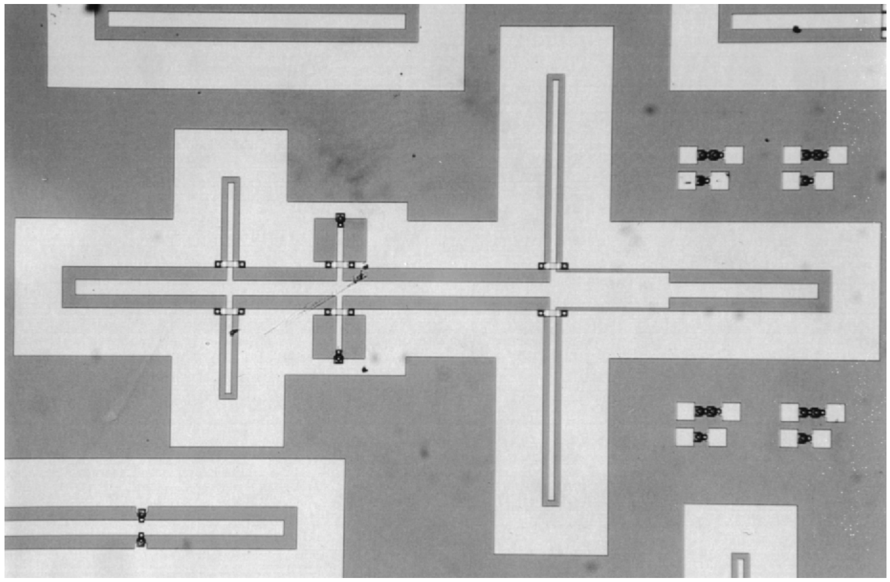

Figure 1. W-Band multiplier.

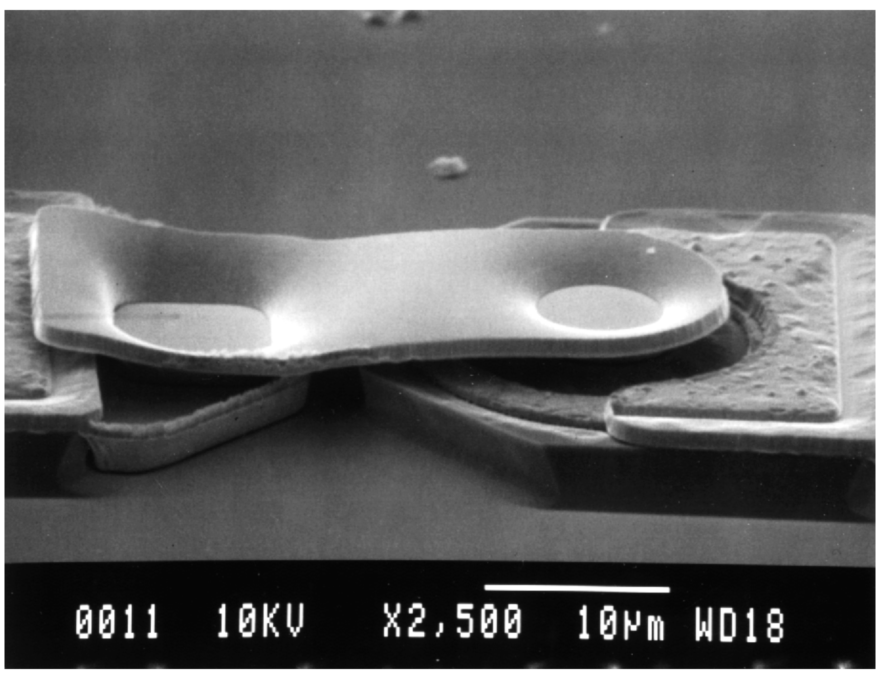

Figure 2. Diode.

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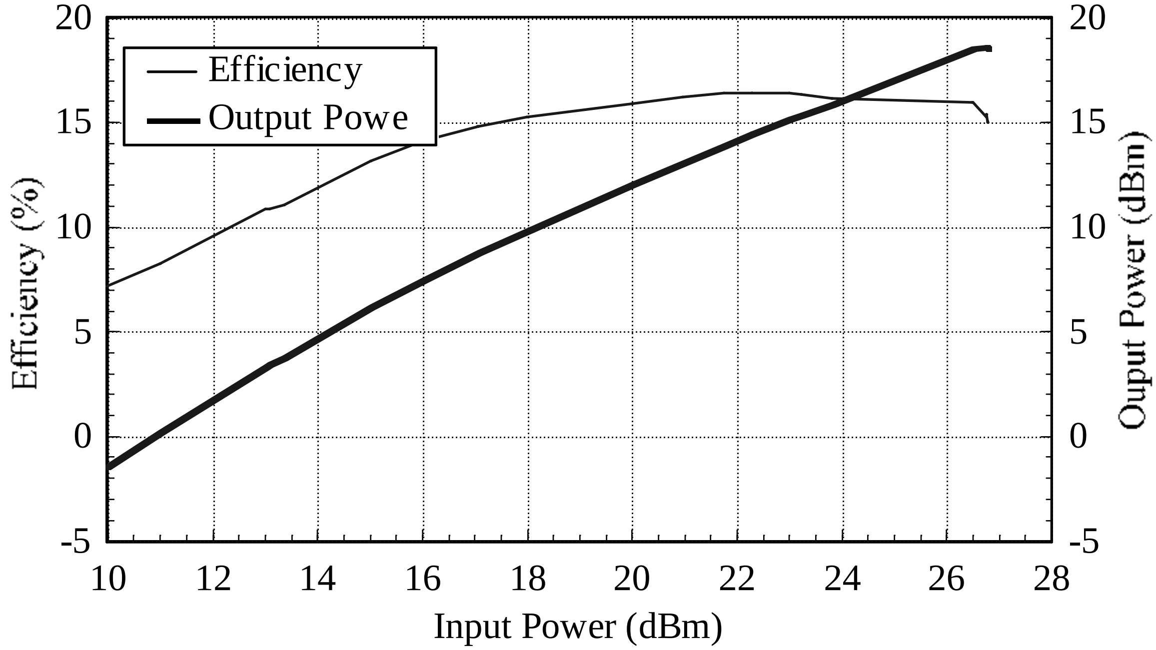

Figure 3. Measured output power and efficiency of the multiplier vs. input power.

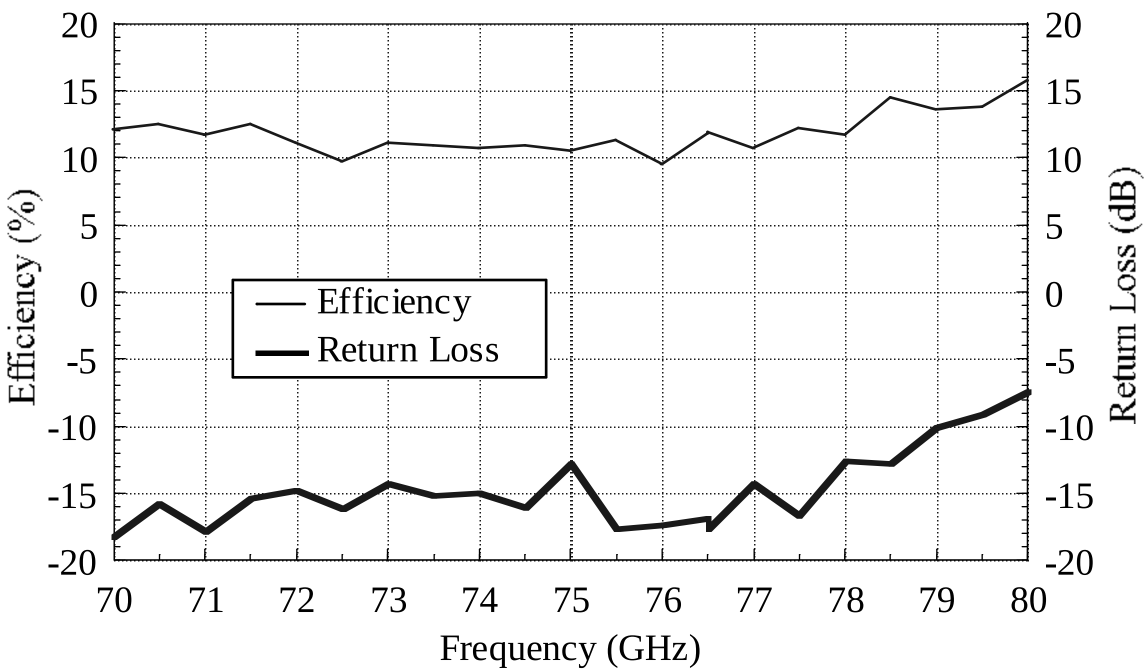

Figure 4. Measured efficiency and return loss vs. frequency.